ELECTRICAL ENGINEERING RELOADED

for Life, Data and Sustainability

The Journey continues in a pandemic year

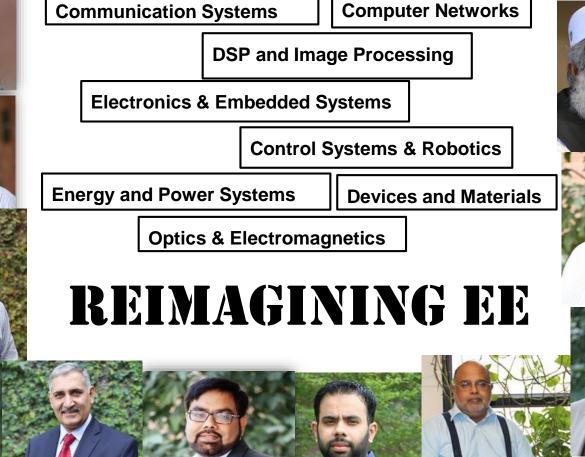
Abubakr Muhammad & the EE Faculty January, 2021

University Education in the 21st century

What would it mean to be human in the age of artificial intelligence, synthetic biology and the Anthropocene?

? Human experience in 21st Century = Life + Data + Sustainability











TENURED

Three tenure applications under review. > 50% will be tenured by end of 2021.

2 Professors11 Associate Professors9 Assistant Professors

r Nauman Butt Dr Hassan Khan









(Data) AI Hardware and Theoretical Foundations (Life) Biomedical Devices and Point-of-Care Healthcare (Sustainability) Systems View of the Water-Energy-Food Nexus

Portable lab kits for online-leaning



EE 324

MICROCONTROLLERS & INTERFACING

Dr. Jahangir Ikram

Each kit contains micro controllers, LED matrix, programmable chips, digital-to-analog converters, an oscilloscope, power distribution core, a complete tool set, a multimeter, speed controllers and motors.

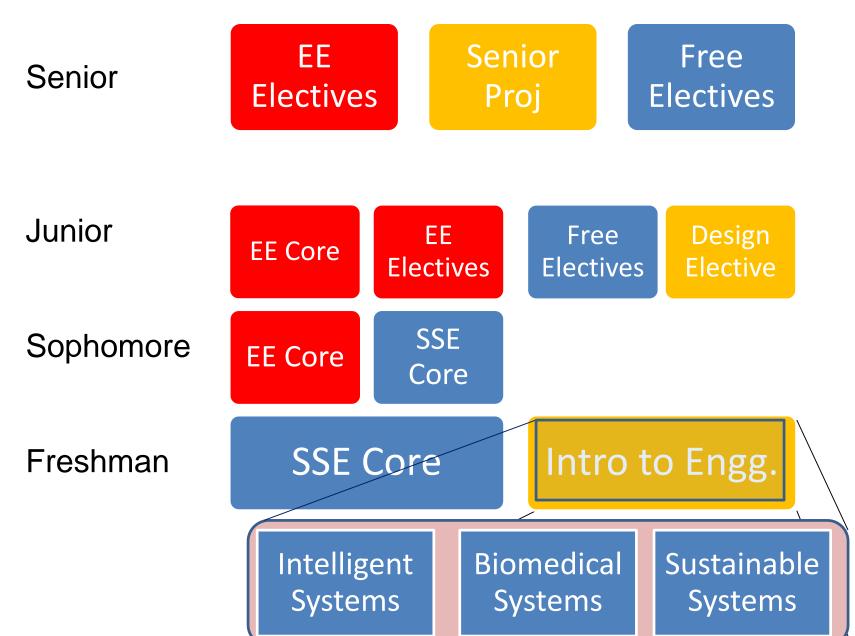
Dr Jahangir Ikram's team developed & shipped **50+ lab kits** indigenously for EE-324.

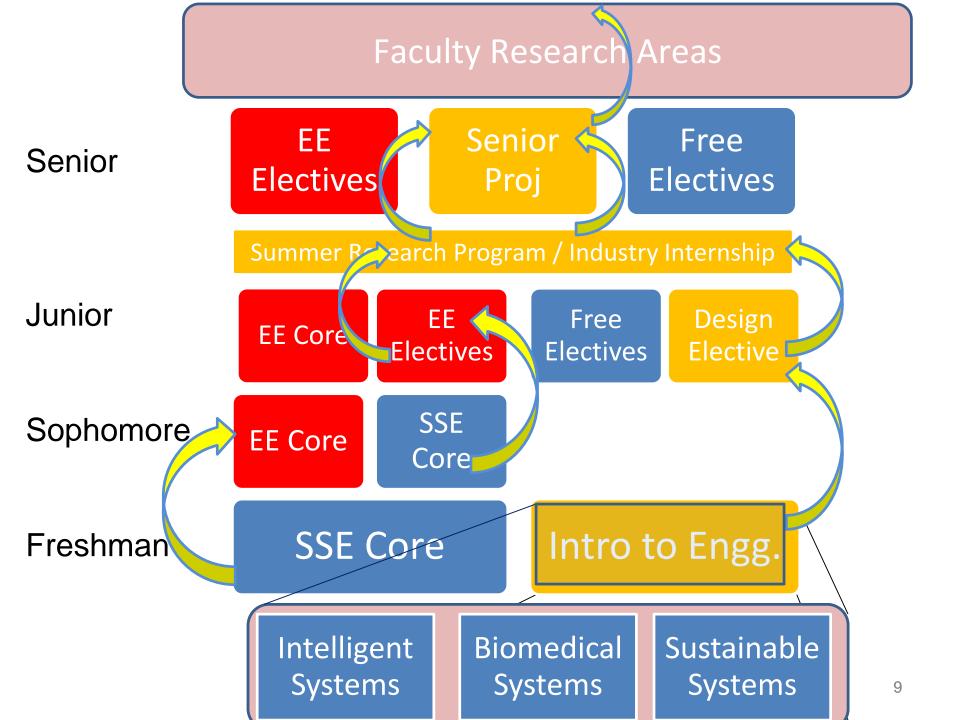
Heroic effort by ALL EE faculty throughout 2020. Minimal damage to teaching & research programs.

Portable lab kits for online-leaning



EE100. The Revolution Begins!





EE-100 Fall 2020: Instructors & TAs



Dr. Momin Uppal



Dr. Abubakr Muhammad



Dr. Muhammad Tahir



Dr. Awais Bin Altaf



Dr. Hassan Jaleel



Dr. Nauman Butt



Dr. Hassan Mohy Ud Din



Eesha Atif EE Senior



Hamza Ather 2020 graduate

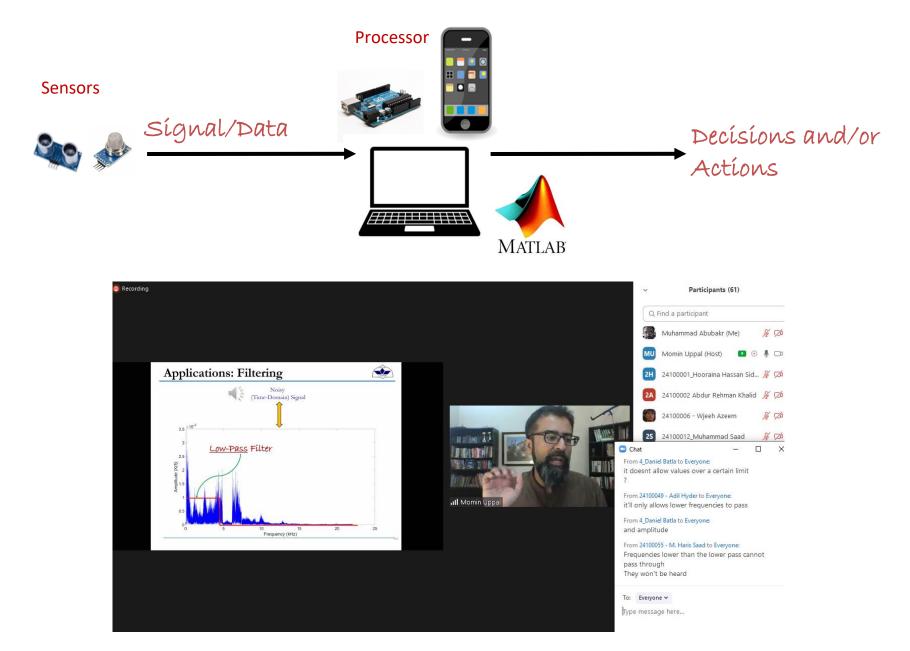


Nouman Arshad Senior Lab Engineer



Syed Hasan Amin Mahmoo 2020 graduate

Content Overview



Student participation



One student group beat a classification accuracy target set by faculty and TAs in their final course project.

Outcomes & Way Forward

- Lab Tasks: Trickle-down of departmental research into freshman teaching
 - Radio Frequency sensing
 - Biomedical signal acquisition
 - Lab-on-a-chip and cell counting
 - Acoustic event detection and localization
 - Intelligent decision-making in agriculture and irrigation

• Spring 2021: Two flavors being offered for EE-100 (1-CH)

- 1. Intelligent systems (Full flavor)
- 2. Sustainable systems (Full flavor)
- Biomedical system (invited lectures)

Transdisciplinary Pedagogical Partnerships

EE 5212/ENGG 342

Syed Babar Ali School of Science and Engineering

FUNDAMENTALS OF BIO NANOTECHNOLOGY

BLENDING BIOLOGY WITH ENGINEERING



Credit Hours | Starting Jan 18, Mon/Wed: 8AM - 9:15 AM

Biology or Material Science background is NOT required

EE 5612 / SCI 302 (WIT Center)

SOCIO-ECOLOGICAL SYSTEMS & SUSTAINABILITY

Dr. Talha Manzoor

EE 557 (Energy Institute)

ELECTRICITY MARKETS

Dr. Hassan A. Khan, Dr. Fiaz Chaudhry

EE 212 (Continuing Education Studies)

MATHEMATICAL FOUNDATIONS FOR MACHINE LEARNING & DATA SCIENCE

Dr. Zubair Khalid

EE 5213 / CS 623 (CS Dept .)

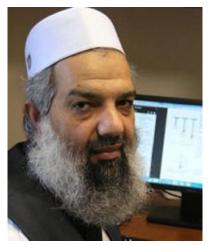
HARDWARE ARCHITECTURES FOR AI

Dr. Rehan Hameed

High Voltage Laboratory Commissioned!







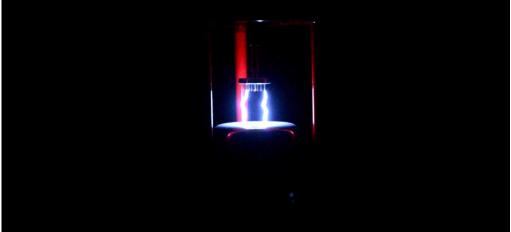
Conceived and designed by: Dr Iqbal Qureshi and Dr Tariq Jadoon





High Voltage Laboratory Commissioned!









EE 553

HIGH VOLTAGE ENGINEERING

Dr. Iqbal Qureshi





Prof. Nauman Zaffar Dr Wasif Khan EE External Relations Committee



Dr Awais bin Altaf



Dr Adeel Pasha









Prof. Nauman Zaffar Dr Wasif Khan EE External Relations Committee

Dr Awais bin Altaf

Dr Adeel Pasha

- Negotiation with multiple organizations for tailored fully funded MS Programs
 - Digital IC Design
 - Intelligent systems
 - Space applications
- One organization has agreed to fund 10x MS students.
- Similar negotiations underway with two others.





Prof. Nauman Zaffar Dr Wasif Khan EE External Relations Committee





Dr Awais bin Altaf

Dr Adeel Pasha

• An Electronics Hardware Accelerator / Technology Fund

- Enabling productization and commercialization of basic research prototypes
- Provide an income source to propel basic research
- ABL has agreed to support the initiative with PKR. 3M for first year.
- Many others have shown interest.







Make in Pakistan Hackathon 2021



Hackathon preparation: (spread over 3 months)

- 9- The winners after the demo of solutions will be offered an

*Dates of different activities will be announced soon.

Connecting centers of entrepreneurship with industries across:









1- Entrepreneurial Ecosystem is growing in Pakistan

2- But Manufacturing industry is losing is competitive edge

3- Manufacturing Industry's Contribution to GDP reduced from 17.5% to 12.5% from 2012 to 2018 4- Pakistani Companies are losing Global Market share

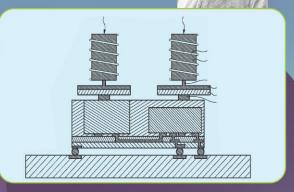
5- To solve the challenges of local industry and to spur innovation, a 16 weeks long project "Make in Pakistan Hackathon: Connecting the Industry to Incubation Centers' is designed

> 16 weeks long project Dav

"Make in Pakistan Hackathon'

🛗 March 27-28, 2021 🔏 NIC, Lahore at LUMS

Patent **Approved!**



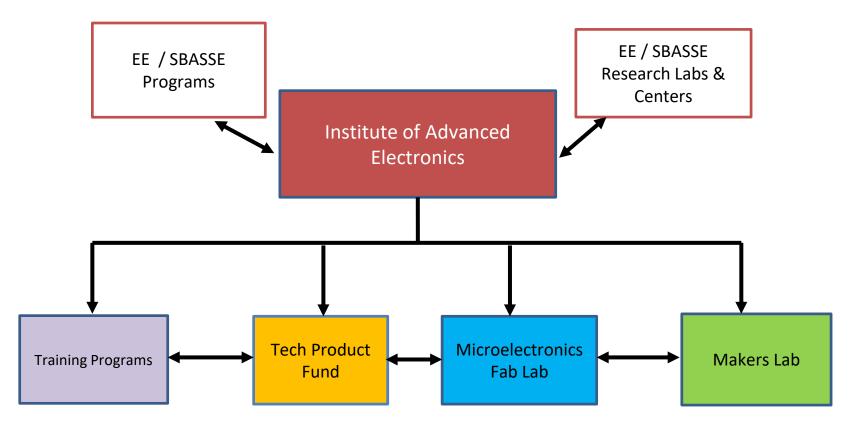
Dr. Wasif Tanveer, an Assistant Professor at Department of Electrical Engineering, just invented a new technology to beam microwaves!

Syed Babar Ali School of Science and Engineering

Dr Wasif Khan (lead) and several others from EE and CS Departments.

miclahore.lums.edu.pk/make-in-pakistan-hackathon-2021/

- Where are we going with this?
 - A future Institute of Advanced Electronics



Student achievements

- Students got placed at MIT two years in a row
- >25% secured funded PhD positions @ top schools
- >80% acceptance rate @ top schools for batch 2020
- 1st Female PhD graduate got post-doc @ Stanford
- No major COVID-impact on employment numbers
 - BS 92% placed after 6 months
 - MS 91% placed after 6 months







Battery-Free Subsea Internet of Things

How a scalable underwater sensor network, which is entirely battery-free, has the potential to monitor the world's oceans.

By Sayed Saad Afzal DOI: 10.1145/3436203

ecently, there has been significant interest in low-power, low-cost scalable underwater networking systems for environmental, defense, and industrial applications. Driven by the need to address the impact of climate change, climatologists and oceanographers are interested in monitoring vital ocean signs such as coral reef conditions, biodiversity, and carbon balance. Similarly, the Defence Advanced Research Projects Agency (DARPA) launched the "Oceans of Things" program

achieving an energy-efficient underwater networking system for maritime situational awareness. On the time, One workaround to this issue is industrial front, top companies, such to use duty cycling where sensors are as Google, Microsoft, and Honey- powered up for only a fraction of the well, seek to deploy such networks to total time, and repeat this process to sors communicate at near-zero power monitor underwater structures ranging from oil and gas pipelines to submerged data centers.

In spite of growing interest and potential in this domain, existing so- tion: Is it possible to create a scalable lutions for a low-cost and low-power distributed underwater sensor network remain largely inadequate. This rates at a considerable operational is because today's underwater systems range? The short answer is yes. rely on point-to-point communication that is power hungry (consuming 50-100 Watts for transmission). As a result, batteries of underwater sensors

62

in 2017 to move toward their goal of get drained quickly. They would need that employs "backscatter," which alout of energy, which limits their lifetransmit data. However, this approach will severely limit our throughput to a measly ten bits per second.

So that leads to the following quesunderwater sensor network that is entirely battery-free, yet offers high data

COMMUNICATING WITH BACKSCATTER Student researchers at MIT have developed an underwater sensor design

120uW to 500uW) than traditional underwater communication systems (see Figures 1 and 2). Backscatter senby simply harvesting energy from ambient signals in the environment and then reflecting them back for communication. This makes them an ideal choice for ultra-low-power networks. Unfortunately, existing backscatter systems work with radiofrequency signals and these signals quickly attenuate underwater, which means these systems cannot be used for underwater communication or power harvesting. Instead, our sensors rely on acoustic signals for backscatter,

lows for communication with 1 mil-

lion times less power (ranging from

XRDS - WINTER 2020 - VDL.27 - ND.2

Sayed Saad Afzal

EE Graduate 2018 batch – Gold Medalist PhD Candidate, Fall 2019, Massachusetts Institute of Technology, USA

■ Menu Weekly edition Economis

Q Search ~

Good vibrations

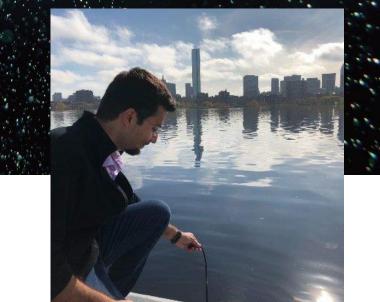
Science & technology Oct 17th 2020 edition >

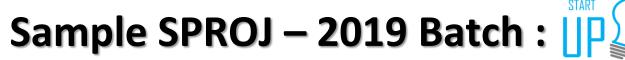
The

How to send underwater messages without batteries

A new device extracts energy from ambient noise







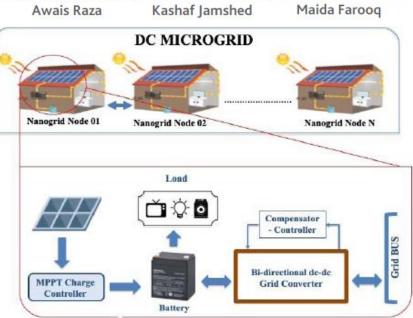
High Voltage Conversion, Bi-Directional DC Microgrid



Prof. Nauman Zaffar



Dr. Hassan Abbas Khan



Simulation / Design (Diagram)

CORRELATING IMAGERY FROM THE SKY THE LUMS AND THE EARTH USING MACHINE A Not-for-Profit University LEARNING PhD work emanating from SSE PHD IN SYED BABAR ALI SCHOOL OF SCIENCE AND ENGINEERING: "19 STUDENTS" **GRADUATE IN 6 MONTHS FROM** ALL DEPARTMENTS. REVOLU Classes **MUSIC OF THE SPHERES:** Freeway FROM PLACENTAL CELLS TO EDGE Mountain Palace Wajeeha Nafees defends her doctoral work on acquiring CANCER TARGETING DRUGS River AND INVENTION Ship signals from spherical sources and novel techniques of Stadium representing them. LUMS Syed Babar Ali School of Science and Engineering

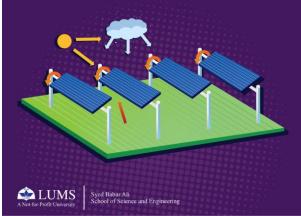
EE PhD graduates in 2020

Saad Zia Sheikh (Dr Adeel Pasha) Muhammad Kamran (Dr Faryad) Numan Khurshid (Dr Murtaza Taj) Wajeeha Nafees (Dr Zubair Khalid) Hassan Imran (Dr Nauman Butt)

AGRIVOLTAICS: THE SUN FOR FOOD

HASSAN IMRAN'S PHD WORK FOCUSES ON DESIGN OF SOLAR CELLS AND INTEGRATING THEM FOR ENHANCING AGRICULTURAL PRODUCE.

Syed Babar Ali School of Science and Engineerin



Micro Doppler Signatures and Multi-Antenna Radars: Research Directions, Challenges and Opportunities Dr. Ijaz Haider Naqvi (Associate Professor, LUMS) and Dr. Faran Awais Butt (Assistant Professor, UMT, Lahore)

Seminar TalK (Online) Dec 07, 2020, 05:30 PM Pakistan Standard Time



Syed Babar Ali School of Science and Engineering



LUMS Department of Electrical Engineering

Dr. Imran Cheema





PhD student excellence

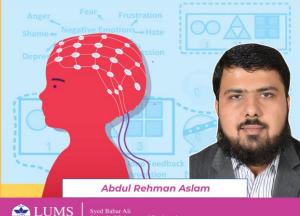




Dr. Awais Bin Altaf

Syed Babar Ali Research Awards

Tracking human emotions



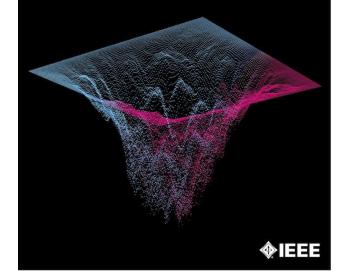
Selected Research Highlights

November 2020 | Volume 108 | Number 11

Proceedings EEE

SPECIAL ISSUE **Optimization for Data-Driven** Learning and Control

Scanning Our Past: The Bell Versus Gray Telephone



INVITED PAPER

Distributed Optimization for Robot Networks: From Real-Time Convex Optimization to Game-Theoretic Self-Organization

This article presents a collection of state-of-the-art results for distributed optimization problems arising in the context of robot networks, with a focus on two special classes of problems. namely, real-time path planning for multirobot systems and self-organization in multirobot systems using game-theoretic approaches.

BY HASSAN JALEEL[®], Member IEEE, AND JEFF S. SHAMMA[®], Fellow IEEE

ABSTRACT Recent advances in sensing, communication, and game-theoretic approaches. For multirobot path planning,

Manuscript received December 22, 2019; revised May 3, 2020 and August 25, 2020: accepted September 17, 2020. Date of current version October 27, 2020.

Systems (IMaSS) Laboratory, Department of Electrical Engineering, Syed Babar All School of Science and Engineering, Lahore University of Management Sciences (LUMS), Lahore 54792, Pakistan (e-mail: hassan Jaleel@iums.edu.pk).

Johnson Lobray, samod service, reaction termine, toward, participation participation, and a service the abolics, intelligent Systems, and Coetrol (RISC) Laboratory, Computer, Electrical and Mathematical Sciences and Engineering (CEMSE) Division, King Abdullah University of Science and Technology (CAUST), Thuwal 23955-6900, Saudi Arabia (e-mali:

(Corresponding author: Jeff S. Shamma.) Hassan Jaleel is with the Intelligent Machines and Sociotechnica

Digital Object Identifier 10.1109/IPBOC 2020 3028295

jeff.shamma@kaust.edu.sa)

computing technologies have enabled the use of multirobot we will present some recent approaches that are based or systems for practical applications such as surveillance, area approximately solving distributed optimization problems over mapping, and search and rescue. For such systems, a major continuous and discrete domains of actions. The main idea challenge is to design decision rules that are real-time- underlying these approaches is that a variety of path planning implementable, require local information only, and guarantee problems can be formulated as convex optimization and subsome desired global performance. Distributed optimization modular minimization problems over continuous and discrete provides a framework for designing such local decision-making action spaces, respectively. To generate local update rules that rules for multirobot systems. In this article, we present are efficiently implementable in real time, these approaches a collection of selected results for distributed optimization rely on approximate solutions to the global problems that can for robot networks. We will focus on two special classes still guarantee some level of desired global performance. For of problems: 1) real-time path planning for multirobot sys- game-theoretic self-organization, we will present a sampling tems and 2) self-organization in multirobot systems using of results for area coverage and real-time target assignment. In these results, the problems are formulated as games, and online updating rules are designed to enable teams of robots to achieve the collective objective in a distributed manner.

> KEYWORDS | Convex functions: distributed algorithms: multirobot systems: optimization.

I. INTRODUCTION

In multirobot systems, a group of individual robots seeks to achieve a collective objective [1]. Motivating applications include collaborative missions, such as exploration [2], area coverage and monitoring [3], [4], task allocation [5], transport [6], and pursuit evasion [7], [8], as well

0018-9219 © 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission See https://www.ieee.org/publications/rights/index.html for more information.

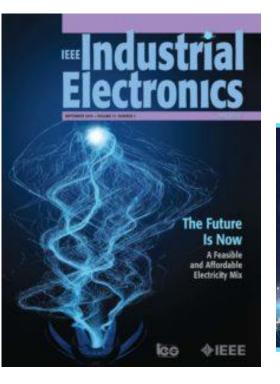
Vol. 108, No. 11, November 2020 | PROCEEDINGS OF THE IEEE 1953

Authorized licensed use limited to: LAHORE UNIV OF MANAGEMENT SCIENCES. Downloaded on October 31,2020 at 10:37:28 UTC from IEEE Xplore. Restrictions apply.



Dr. Hassan Jaleel

Selected Research Highlights



Blockchain Technologies for Smart Energy Systems

Fundamentals, Challenges, and Solutions



chain-based smart energy projects

in different domains. The majority of

blockchain platforms with embedded

combination of blockchain technol-

ogy solutions are computing- and

resource-intensive and, hence, are

not entirely suitable for smart en-

ergy applications. We consider the re-

quirements of smart energy systems

and accordingly identify appropri-

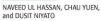
ate blockchain technology solutions

for smart energy applications. Our

analysis can help in the development

of flexible blockchain platforms for

smart energy systems.



n this article, we discuss the integration of the blockchain into smart energy systems. We present various blockchain technology solutions, review important blockchain platforms, and describe several block-

Digital Object Mentifier 10 1109/MIE 2019 2940325 Date of current version: 23 December 2019

106 IEEE INDUSTRIAL ELECTRONICS MAGAZINE EDECEMBER 2019

The Potential for **Blockchain Applications**

The continuous expansion of smart energy systems for industrial, commercial, and domestic applications presents several new challenges and opportunities [1], [2]. Smart infrastructure (SI), renewable energy sources (RESs), and electric vehicles (EVs) are becoming widespread [3], [4]; energy and carbon trading possibilities are increasing [5]-[7]; and energy management (EM) through demand-response management (DRM) programs is becoming more common

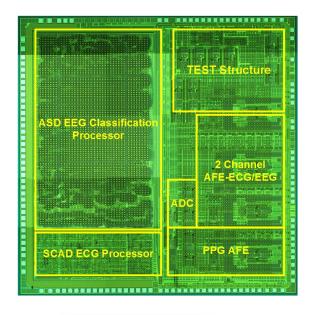
1932-4529/19@2019IFFF



Dr. Naveed ul Hassan

Selected Research Highlights

	Implemented Results	
	Process	TSMC 0.18um 1P6M CMOS
Classification	Area	4.0 x 4.0 mm
S a Classification	Supply Voltage	1.0V (AFE) 1.0V (DBE)
	NEF/channel	2.71
	Classifier	DNN
	Energy Efficiency	10.13uJ/Class.
ST-Struct 2-ch-AFE ADC S ADC 	Accuracy	85.2%
TEST Struct 2-ch-AFE ADC BLAS BLAS BLAS CTDC C-TDC ADC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-TDC C-Ch-AFE C-CH-AFE	No. of Classes	4
	PS Weight Memory	16KB



.0			Implemen	ted Results	
<u>c</u> /	*****	LED	Process	180nm	
NMG-SVR FE Engine ALDCU	NMG-SVR	Driver	Technology	NIR-PPG with NMG-SVM	
	PPG	Area	2.0 x 3.0 mm ²	-	
		Readout	Supply	1.1V	600um
		Power	186µW	З	
	Ingino	SAR ADC	Duty Cycle	0.125%	
	ALDCU		I _{in, maxDC}	65µA	
	Test	Integrated RTI Noise	9.4pA _{rms}		
	Test		Gain	120dB	
			mARD	5.2% (200 Subjects)	

	Process	0.18µm 1P6M
Feature Extraction Extraction PAFARL	Active Area	0.3 x 0.6mm
	Supply Voltage	1.0 V
	# of CA	8
Multi-CA ECG Classifier	Power	1.536uW @ 1KHz
	Accuracy	98.5%
300um		





First ever indigenous chip design and tape out from Pakistan.

IEEE Journal of Internet of Things

IEEE TRANSACTIONS ON

CIRCUITS AND SYSTEMS EXPRESS BRIEFS

POCUSING ON ALL MATTERS BELATED TO FUNDAMENTAL THEORY. APPLICATIONS ANALOG AND DIGITAL SIGNAL PROCESSING

A Volunteer Supported Fog Computing Environment for Delay-Sensitive IoT Applications

Bahar Ali, Muhammad Adrel Parket Carine Manther IEEE Care a Line Houbing Song, Senior Member, 3407

Abstract-Fog Computing (FC) has emerged as a co-mentary solution to the centralized cloud infrastructure FC node is available in closer previnity to users and ex-cloud services to the edge of the network in a highly distri manner. However, with an increase in streaming and sensitive Internet of Things (IoT) applications, FC also to address the issue of higher latency while forwarding com intensive jobs to remote cloud data centers. Hence, there is a to investigate the use of computational resources at the ed the network. Volunteer Computing (VC) offers a reduction the network containing high-performance computing by makin of user-owned underutilized or tide resources, e.g., haptop desktog computiers closer to fag devices. We propose Vola Supported Fog Computing (VSFC), as a computing para that explores the interplay of these two distributed comp domains to help minimize inherent communication dela cloud computing, energy consumption, and network usag this effect, we have extended the iFogSim toolkit to su VSFC, Extensive simulations show that VSFC outperforms tional FC-cloud computing by reducing delay by 47.5%, e by 93%, and network usage by 92% under normal to heavy

Index Terms—Distributed Computing Paradigms, Intern Things, Fog Computing, Volunteer Computing, Cloud Co-ing, Resource Management

I INTRODUCTION

The plethora of smart devices has encouraged the indu and research communities to envision the beauty of predi and taking precautionary measures in advance to save p of resources. In this regard, the Internet of Things supports the phenomenon of connecting every object o face of Earth irrespective of its platform, communic technology, etc. [1]. The IoT environment comprises of t that can be your wearables (smartwatch, glasses, etc.), vel (autonomous cars, smart bikes, etc.), fun time gadgets

Manuscript monived April 16, 2020; revised July 23, 2020; accepted XX, 20XX. Date of publication XXX XX, 20XX; date of current XXX XX, 20XX.

Habar All is with the Department of Computer Science, SIA Science and Engineering, Labour University of Management Sc 2005), 54792, Labour Pakistan, e-mail: 17030033491umcodu.pk. Abbay Set 24, Labor Partian e-mail: reconcilentation pit, Muhammad Arkel Paulu with the Department of Blochical Bagin (A. School of Science and Engineering, Labor. University of Mang sciences (LUMS), 54792, Laborab Pakitan e-mail: aideo packad Barna, Saif al-blam is with the Department of Computer Science, Indi

Space Technology, Islamahad, Pakistan. e-mail: saithu2004@gmail.com Houbing Song is with the Department of Electrical Engineerin Computer Science, Embry-Riddle Aeronautical University, Daytona 1 FL 32114 USA, e-mail: hsong@kees.org Rajkamar Buyya is with Cloud Compating and Distributed 5

(CLOUDS) Laboratory, School of Computing and Information Syste University of Melbourne, Parkville, Australia e-mail: rhuyya@unimelb

Matrix-Matrix Multiplication for CNNs on FPGAs Afzal Ahmad^O and Muhammad Adeel Pasha^O Abstract-Convolution is inarguably the most complex Convnet architectures for mobile vision applications are focusing on decreasing the cost of convolutional (conv) layers due to their high computation complexity. Modern state-of-the-art convnets for mobile vision applications are utilizing

Optimizing Hardware Accelerated General

BUD TRANSACTIONS ON CIRCUITS AND SYSTEMS-IE DOPRIES BRIDES, VOL. 67, NO. 11, NOVEMBER 2020

aimed at improving accuracy.

depthwise, pointwise, and grouped convolutions to reduce

network complexity and model size while maintaining high

accuracy [1], [2]. Unfortunately, research in convnet archi-

tectures for mobile vision applications is not proceeding as

rapidly as research in denser and more complex convnets

Therefore, as modern convnets tend towards deeper topolo-

gies trained on large datasets, there is a need to design efficient

hardware accelerators that meet both energy and real-time

computation constraints for mobile vision applications. In

this brief, we design an FPGA-based accelerator for general

matrix-matrix multiplication (GeMM), a key operation utilized

extensively in convnets. As a use-case, we apply our accel-

erator to improve the performance of convolutional (conv)

layers of Shufflenet-v1 [2], an efficient convnet architecture.

· We design an FPGA-based hardware accelerator for

GeMM by pipelining and parallelizing computational

We optimize our hardware accelerator to map conv layers

We compare the performance of our accelerator system with several state-of-the-art FPGA-based solutions for

both high-complexity and efficient convnet architectures.

II. RELATED WORKS

accelerator for SSIDLIteM2, utilizing several hardware opti-

mizations, and achieving 65 frames per second (fps) on a

Zynq-7000 SoC. Su et al. [4] proposed redundancy-reduced

mobilenet, yielding significantly lower memory and com-putational complexity of the model compared to baseline

mobilenets [1], and achieving inference time of only 7.85 ms

an accelerator system for depthwise separable convolution,

achieving 17.6× speedup over a TitanX GPU-based imple-

mentation. Xiao et al. [6] proposed a fusion architecture to fuse layers of convnets to allow reuse of intermediate data

while also utilizing Winograd minimal filtering to reduce

resource utilization, testing their design on both VGG16 and Alexnet. Moini et al. [7] proposed a resource-efficient accel-

erator, exploiting parallelism and reuse to reduce bandwidth,

efficient convnet architectures - including standard, grouped

Owing to different types of convolutions involved in these

resource, and power consumption.

Fan et al. [3] designed an FPGA-based object-detection

of Shufflenet onto the GeMM engine efficiently.

The main contributions of this brief are as follows:

workload across available resources.

Astract-Convolution is marguary the new compet-operation utilized in Convolutional Neural Networks (convects), Owing to the billions of independent multiply-adds involved, convolution is being massively parallelized by the simultane-ous utilization of many cores of Graphical Processing Units (GPUs). Although GPUs have shown significant performance improvements in both training and inference stages, they are not well-suited for mobile vision applications where both energy and real-time constraints need to be satisfied. In contrast, Field Programmable Gate Arrays (FPGAs) have demonstrated massive parallelization capabilities, with fast DSPs and on-chip memory, at a lower energy cost than GPUs. Hence, they are being utilized to design convnet accelerators for embedded appliusing unitate to using connect accurators in timeorate appli-cations. In this brief, we design an FPGA-based accelerator for general matrix-matrix multiplication (GeMM) to improve the efficiency of convolutional layers of ShuttBined, an effi-cient convnet architecture. Experimental results show significant performance improvements against the state-of-the-art FPGA-based implementations of both difficult convertises that are tailored towards mobile vision applications, and complex convnets that are used in traditional applications.

Index Terms-Hardware acceleration, FPGAs, convnets.

I. INTRODUCTION

- ONVOLUTIONAL Neural Networks (convnets) have established themselves as the de-facto standard for several applications in the domain of computer vision such as image classification, object detection, semantic segmentation, and generative modeling. While the accuracy of convnets is improving at an unprecedented rate owing to the increasing ability to train deeper networks with larger datasets, their computational complexity is proportionally increasing to meet the demands for improved accuracy for use in critical applications such as self-driving vehicles. Graphical Processing Units (GPUs) have demonstrated high performance on convnets due to their parallelization capabilities, but their generality and high power consumption limit them. One the other hand, Field Programmable Gate Array (FPGA)-based hardware accelerators are being utilized to design convnet architectures, exploiting their massively parallel and pipelined logic resources, and on an UltraScale+ IPGA platform. Ding et al. [5] designed fast on-chip memory

Manuscript received December 17, 2019; accepted January 3, 2020. Date of publication January 9, 2020; date of current version November 4, 2020. This hold was accommoded by Associate Biller CC W. Slass (Corresponding audwor: Mulanesual Adorf Units). The audwors are within Department of Electrical Higgsnoring, Synd Thiler Advisors, Labore S4702, Engineering, Labore University of Management Sciences, Labore S4702, Engineering, Labore University of Management Sciences, Labore S4702, Fingheomite, Const. at adv. Antel Wann and Jeff

adocl.copha@lams.odu.ck) Color ventions of one or more of the ligares in this article are available tilter at http://soenciore.looc.org.

line al http://ieeexplore.ieee.org. Digital Object Identifier 10.1109/TCSII.2020.2965154

1549-7747 (§) 2020 II202. Personal use is permitted, but republication/redistribution requires IE202 permission. Soc https://www.ioze.org/publications/rights/index.html for more information.

ACM Transactions on **Embedded Computing** Systems

LETELETTERS OF THE COMPUTER SOCIETY, VOL. 3, NO. 2, JULY-DECEMBER 2020

A Dynamic Cache-Partition Schedulability Analysis for Partitioned Scheduling on Multicore Real-Time Systems

Saad Zia Sheikh ⁽²⁾, Student Member, IEEE and Muhammad Adeel Pasha ⁽³⁾, Senior Member, IEEE

Abstract—Recent Integration of the cache-partition model has usbarred in new paradigms of measurch in the predictability and achedul ability analysis for real-time systems. However, simplicity in the analysis transpork has prompted existing ontributions to be biased towards a static cache-partitioning scheme The dynamic scheme has largely been untadied depile is profilency in scheduability, fexibility, and energy-efficiency. In this letter, we address th problem and make initial contributions to a dynamic cache-partition achedul ability analysis for multicone partitioned acheduling of easi-line fixed-priority aporadic tasks. We device a sufficient achedulability jest and then either the upper-bound by proposing techniques to induce the pessinium in the interference caused by ache contenton

nd global re in the

there pro-

by bests to on into m

due to t

uests max

troduce

ared cach

roposed

from th

ections d

prevent

che parti reCPsas

tion, and

red at run

the ma

focus or

s since

td are ra

ing on c

e analysis

non-time o

ty [1]. H

esources. mber of c

e the nur

e cache a

ach core.

ctrical Engli weity of M D, adel pari

July 2020; 1 1 38 Aug. 2

10301564

10000 20201

barbaria.



to have an adverse impact on the energy-efficiency of the system and attempts have been made to adopt a dynamic CP scheme into

partitioned scheduling where the CPs are dynamically allocated to the cores. However, such initiatives are limited to simpler framebased tasks [2] and integer linear program (ILP) formulations [3]. The dynamic CP scheme has been exclusively used in global scheduling. In traditional global scheduling, tasks are dynamically allocated to cons. This can theoretically increase the schedulability. owever, schedulability tests for global scheduling algorithm

largely pensimistic since the critical instant of a task tasks (HPTs) will lead to the maximum response t mined via the problem mindow approach, where a j assumed to have missed its deadline and the ma then used to determine its schedulability [4]. These # Sciences, Pakistan ability tests have been extended into the CP-scenari

FFConv: An FPGA-based Accelerator for Fast Convolution Layers in Convolutional Neural Networks

AFZALAHMAD and MUHAMMAD ADEEL PASHA (LUMS), Pakistan

Image classification is known to be one of the most challengin Significant research is being done on developing systems and a area, and power consumption for related problems. Convolution give outstanding accuracies for problems such as image classed mentation. While CNNs are pioneering the development of high tional complexity presents a barrier for a more permeated deploy (GPUs), due to their massively parallel architecture, have shown ter than general purpose processors, the former are limited by th Consequently, Held Programmable Gate Arrays (FPGAs) are bei as they also provide massively parallel logic resources but with GPUs. In this article, we present FFCony, an efficient FPGA-be CNNs. We design a pipelined, high-throughput convolution en ing (also called Fast Convolution) algorithms for computing the architectures VGG16, Alexnet, and Shufflenet. We implement o where we exploit the computational parallelization to the maxi improving performance. The resultant design loses only 0.43%, 0. for VGG16, Alexnet, and Shufflenet-v1, respectively, while signif power efficiency compared to previous state-of-the-art designs.

CCS Concepts: • Hardware -> Hardware accelerators:

Additional Key Words and Phrases: FPGA, convolutional neural

ACM Reference format:

Afzal Ahmad and Muhammad A deel Pasha, 2020, FFConv: An FF

Layers in Convolutional Neural Networks. ACM Trans. Embed. (

24 pages

https://doi.org/10.1145/3380548

1 INTRODUCTION

With the advent of Artificial Intelligence (AI), the popularity of Departa Adeel Pasha pattern recognition to natural language processing. Convolutional Neural Networks (

Authors' addresses: A. Ahmad and M. A. Pasha, Department of Electrical Engineering, Lahore University of Management Sciences (LUMS), Labore, Pakistan; emails: (afcal.ahmad, adeel.pasha)@lums.edu.pk. Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyrights for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee. Request permissions from permissions@acm.org. @ 2020 Association for Computing Machinery. 1539-9087/2020/03-ART15 \$15.00

ACM Transactions on Embedded Computing Systems, Vol. 19, No. 2, Article 15. Publication date: March 2020.

https://doi.org/10.1145/3380548

IEEE LETTERS OF THE COMPUTER SOCIETY



i.e., it is unknown which specific sequence of its | Energy-efficient Real-time Scheduling on Multicores: an upper-bound on the interference from HPTs A Novel Approach to Model Cache Contention

ence from its HPTs, that led to its deadline miss, it SAAD ZIA SHEIKH and MUHAMMAD ADEEL PASHA, Labore University of Management

idoption of multicores has been a major stepping the computational bandwidth is increased due to the hierarchical memory sub-system and multiple use execution time (WCET) analysis of tasks. Puron time, and the inclusion of shared caches further



15

Survived the Pandemic. Where to Next?

- Build on EE100 success.
- Industry partnerships for alternative funding streams.
- Space and HR constraints for major initiatives.
- BS and MS Student numbers
- Pedagogical partnerships
- Niche PhD and postdoctoral programs.
- Tenured faculty needs to think big!

	Session	BS Students
	2019	46
or	2020	43
	2021	56
	2022	46
	2023	40

The EE revolution marches on!

Thank you.